AMENDMENTS TO THE CLAIMS

Claims 1 – 31. (canceled)

32. (original) A method of forming a CMOS imager having improved charge storage comprising the steps of:

providing a semiconductor substrate having a doped layer of a first conductivity type;

forming a first doped region of a second conductivity type in said doped layer, said first doped region being adjacent a field oxide region;

forming a charge storage capacitor overlying entirely over at least one of said field oxide region and an active area of said CMOS imager; and

forming a contact between said first doped region and said charge storage capacitor, a storage capacity of the capacitor being selected based on the color of the photosensor.

33. (currently amended) The method according to claim 32 ~~35~~, wherein said charge storage capacitor is formed entirely over said field oxide region.

34. (currently amended) The method according to claim 32 ~~35~~, wherein said charge storage capacitor is formed entirely over said active area.

35. (currently amended) The method according to claim 32 ~~35~~, wherein said charge storage capacitor is formed by:

forming a first conductive layer over said substrate including said field oxide region;

forming a dielectric layer over said first conductive layer; and

forming a second conductive layer over said dielectric layer.

36. (currently amended) The method according to claim 35 ~~38~~, wherein said first electrode is a titanium nitride layer, a doped polysilicon layer or a hemispherical grained polysilicon layer.

37. (currently amended) The method according to claim 35 ~~38~~, wherein said second electrode is a platinum metal layer, a tungsten metal layer, a titanium nitride layer or a doped polysilicon layer.

38. (currently amended) The method according to claim 35 ~~38~~, further comprising:

forming a second doped region of said second conductivity type in the doped layer spaced from said first doped region to transfer charge from a charge collection area;

forming a third doped region of said second conductivity type in the doped layer spaced from said second doped region wherein said third doped region effectuates the transfer of charge to a readout circuit; and

forming a fourth doped region of said second conductivity type in the doped layer spaced from said third doped region wherein

said fourth doped region is a drain for a reset transistor for said CMOS imager.

39. (currently amended) The method according to claim 38 ~~42~~, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

40. (currently amended) The method according to claim 38 ~~42~~, further comprising forming a photogate over said doped layer between said first and second doped regions.

41. (original) A method of forming a CMOS imager having improved charge storage comprising the steps of:

providing a semiconductor substrate having a doped layer of a first conductivity type;

forming a field oxide region within said semiconductor substrate;

forming a first conductive layer over said field oxide region and said substrate;

forming an insulating layer over said first conductive layer;

forming a second conductive layer over said insulating layer;

patterning said first conductive layer, said insulating layer and said second conductive layer to form a storage capacitor and an electrical element of said CMOS imager, wherein said storage capacitor is formed entirely over and in contact with said field oxide region, a storage capacity of the capacitor being selected based on the color of the photosensor.

42. (currently amended) The method according to claim 41 [[44]], further comprising:

forming a first doped region of a second conductivity type in said doped layer and adjacent said field oxide region;

forming a second doped region of said second conductivity type in said doped layer spaced from said first doped region;

forming a third doped region of said second conductivity type in said doped layer spaced from said second doped region and adjacent said electrical element; and

forming a fourth doped region of said second conductivity type in said doped layer spaced from said third doped region.

43. (currently amended) The method according to claim 42 ~~45~~, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

44. (currently amended) The method according to claim 43 ~~46~~, wherein said first doped region, said second doped region, said third doped region and said fourth doped region are doped at a dopant concentration of from about $1x10^{15}$ ions/cm^2 to about $1x10^{16}$ ions/cm^2.

45. (currently amended) The method according to claim 44 ~~47~~, wherein said electrical element is a transfer gate.

46. (original) The method according to claim 45, further comprising forming a reset transistor and a source follower transistor.